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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/505,431	08/24/2004	Katsutoshi Moriyama	SON-2624	1635

23353 7590 05/23/2007

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EXAMINER	
ELAND, SHAWN	
ART UNIT	**PAPER NUMBER**
2188	

MAIL DATE	DELIVERY MODE
05/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/505,431	MORIYAMA ET AL.	
	Examiner	Art Unit	
	Shawn Eland	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5 and 7-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5 and 7-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/20/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Formal Matters

This Office action is in response to the Applicant's response filed on April 20, 2007.

Applicant's response, dated April 20, 2007 states "that the IDS included a typo, inadvertently reciting JPO action ***2002-079529***, instead of JPO action ***2002-079529***." Applicant's response in this regard does not make sense and the Examiner assumes that this is a typo, and perhaps said IDS should have recited JPO action number 2002-079528. The Examiner respectfully requests that Applicant state which JPO action number should have been on said IDS.

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Status of Claims

Claims 1, 3, 5, & 7 – 13 are pending in the Application.

There are no amended or new claims.

Claims 2, 4, & 6 are cancelled.

Claims 1, 3, 5, & 7 – 13 are rejected.

Response to Arguments

Applicant's arguments filed April 20, 2007 have been fully considered but they are not persuasive.

Applicant argues that Searby does not teach or suggest a "circuit" or "device" and instead teaches a system of independent devices where some of the components are "implemented algorithmically." It's well known in the art the systems are implemented by circuits. Circuits and devices are both known in the art as hardware. Searby cannot run on software alone. While Searby teaches some devices ***may*** be integrated with the circuit, Applicant's claim language does not specifically exclude integration of third party devices within its circuit. It is also notoriously well known in the art that devices, such as PDAs for example, will utilize third party components, like storage devices, to simplify development and use, and that circuits can be programmed to utilize different algorithms.

Applicant submits that the comparator may be implemented as software and because of this, the inherency argument provided by the Examiner regarding the control signal generating section fails. The Examiner respectfully disagrees. It is perfectly reasonable for a person having ordinary skill in the art to look at Searby and understand that the comparator and other components are utilized in hardware. Whether or not the comparator can be implemented in software was not the argument. If the comparator exists in hardware, it must have a control signal generating section so the circuit will know when to read the control signal image data and brush coefficient.

The readout control section, as claimed, generates a signal to read existing data from the storage element and a signal to write new data to the storage element based on whether or not said signals differ from each other. The Examiner has already stated in the previous Office action dated March 22, 2007 that the control signal generating section is not shown by Searby. Further, Applicant argues that some sections of Searby may be implemented in software. Searby knows when to read the existing data and when to write the new data. As argued in the paragraph above, this section must exist if implemented in hardware, and it is reasonable to assume that Searby is implemented in hardware.

With respect to claim 8, the Examiner does not state that the stylus 7 produces "both a write control and a read control signal." The claim clearly states that these signals are *derived from* a write signal output. Stylus 7 is both a source of new data as well as a source for the write control and read control signals.

Applicant's remaining arguments with respect to the arguments not addressed by the Examiner in the outstanding office action have been considered but are moot in view of the new grounds of rejection.

Hindsight was not used for the 35 U.S.C. 103 rejections. Usage of AND, NOR, and XOR logic gates in circuits were well known in the art at the time the invention was made. The Applicant sites no inventive concept in the use of these gates that was not used or would not have been obvious to one of ordinary skill in the art. There is no unexpected result in using any of these elements and, hence, they are obvious. See ex parte Mead Johnson & Co. 227 USPQ 78.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5, 7 – 8 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Searby*** (US 5,412,402).

In regard to claim 1, Searby teaches a comparison section for reading out existing data stored in a storage element to compare said existing data and new data with each other prior to writing of said new data to said storage element ***(see element 13)***, and configuring so that, in said comparison section, in a case where said exiting data and said new data are identical with each other, the writing to said storage element is not performed, and in a case where said existing data and said new data are not identical with each other, said new data is written to said storage element ***(see column 7, lines 34 – 38;)***; and characterized by provided with a control signal generating section for generating a readout control signal for performing readout control of said existing data and a write control signal for performing write control of said new data ***(the control signal generating section, while not shown, must exist in order for the circuit to know when to read control image data K and brush coefficient K_B)***, and by configuring so that said existing data and said new data are compared with each

other in said comparison section in accordance with said write control signal from said control signal generating section ***(see column 8, lines 13 – 17)***.

Regarding claim 8, Searby teaches wherein said readout control signal and said write control signal are derived from a write signal input to said control signal generating section ***(see element 7)***.

In regard to claim 3, Searby teaches performing a readout process of existing data stored in a storage element prior to performing a write process of new data to said storage element to compare said existing data and said new data with each other ***(see column 7, lines 16 – 21)***, so as not to perform the write process to said storage element, in a case where said existing data and said new data are identical with each other, and so as to perform the write process of said new data to said storage element in a case where said existing data and said new data are not identical with each other ***(see column 7, lines 34 – 38)***; characterized by generating a readout control signal ***(the system has to know when to read out the existing data so therefore it is inherent)*** and a write control signal ***(see column 7 lines 26 – 34)*** in accordance with a write signal input ***(see element 7)*** to said data storage circuit; reading out said existing data in accordance with said readout control signal ***(see column 6, lines 3 – 4)***; and comparing said existing data with said new data in accordance with said write control signal ***(see column 7, lines 34 – 38)***.

In regard to claim 5, Searby teaches a comparison section for reading out existing data stored in a storage element to compare said existing data and new data with each other prior to writing of said new data to said storage element ***(see element***

13), and configuring so that, in said comparison section, in a case where said existing data and said new data are identical with each other, the writing to said storage element is not performed, and in a case where said existing data and said new data are not identical with each other, the writing of said new data to said storage element is performed ***(see column 7, lines 34 – 38)***; characterized by providing with a control signal generating section ***(the control signal generating section, while not shown, must exist in order for the circuit to know when to read control image data K and brush coefficient K_B)*** for generating a readout control signal for performing readout control of said existing data ***(the system has to know when to read out the existing data so therefore it is inherent)*** and a write control signal for performing write control of said new data, and by configuring so that said existing data and said new data are compared with each other in said comparison section in accordance with a control signal from said control signal generating section ***(see column 7, lines 34 – 38)***.

Regarding claim 7, Searby teaches the comparison section is provided with a new data retention section for temporarily retaining the new data ***(see element 14)***; an existing data retention section for temporarily retaining the existing data ***(see element 14)***; and a write enable signal generating section for comparing the new data retained in the new data retention section and the existing data retained in the existing data retention section with each other to control an output of the write enable signal ***(see column 8, lines 23 – 26)***, the new data is temporarily retained in the new data retention section while the existing data is temporarily retained in the existing data retention section in accordance with the readout control signal output from the control signal

generating section, and the new data retained in the new data retention section and the existing data retained in the existing data retention section are compared with each other in accordance with the write control signal output from the control signal generating section ***(see column 7, lines 34 – 38; see column 8, lines 13 – 17)***.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 & 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Searby*** (US 5,412,402) in view of ***Moyer*** (US 6,052,302).

For the claims from which claims 9 & 13 depend upon, see 102(b) rejections over Searby above.

For claim 9, Searby teaches said control signal generating section but does not teach wherein said control signal generating section includes an AND logic gate for generating said readout control signal according to a first readout generation signal and a second readout generation signal. Moyer teaches including AND logic gates. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use this embodiment, as it would help minimize power consumption.

For claim 13, Searby does not teach wherein the write enable signal generation section includes an XOR logic gate for generating a write enable signal in accordance with the new data and the existing data. However, Moyer does ***(see figure 7)***. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use this embodiment, as it would help minimize power consumption.

Claims 10 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Searby*** (US 5,412,402) as applied to claim 9 above, and further in view of ***Kunikiyo*** (US 2002/0145902).

For the claims from which claims 10 – 12 depend upon, see 102(b) rejections over Searby above.

For claim 10, Searby does not teach wherein said control signal generating section includes a NOR logic gate for generating said write control signal according to a first write generation signal and a second write generation signal. However, Kunikiyo does ***(see [0390])***. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use this MRAM, as it would reduce the amount of time taken for batch erasing.

For claim 11, Searby does not teach wherein said new data retention section and existing data retention section include input control transistors for controlling the retaining of the new data and the existing data in accordance with readout control signal. Kunikiyo, however, does ***(see [0092])***. It would have been obvious to a person

having ordinary skill in the art at the time the invention was made to use this MRAM, as it would reduce the amount of time taken for batch erasing.

For claim 12, Searby does not teach wherein the write enable signal generation section includes output control transistors for controlling comparison of the new data and the existing data in accordance with the write control signal, but Kunikiyo does ***(see [0092])***. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use this MRAM, as it would reduce the amount of time taken for batch erasing.

Examiner's Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Eland whose telephone number is (571) 270-1029. The examiner can normally be reached on MO - TH, & every other FR.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SE

Shawn Eland
05/16/07

HYUNG SOUGH
PATENT EXAMINER
5-17-07